# Ansys VeloceRF

## The Most Complete and Efficient Spiral Inductor, Transformer, and Transmission Line Device Compiler

- Enables synthesis of complex spiral topologies and transmission lines according to user-defined electrical and physical specifications.

- Delivers DRC-clean and DfM-correct parametric cells for any process node down to 3nm.

## Key Features

- Synthesizes DRC-clean/DfM-correct devices by design down to 3nm CMOS

- Rich and sophisticated parametric cells with unrivaled flexibility in parameterization

- Support of parametrized ground shield and dummy fill as PCell options

- Optimized for silicon

- Various output formats for maximum efficiency in circuit simulation

- Compatible with all IC design platforms, physical verification flows, and circuit simulators

- Silicon-accurate

## Meet Your Most Demanding Inductor Requirements

Ansys VeloceRF™ is powerful software that synthesizes complex spiral structures and transmission lines in real-time based on your own electrical and physical specifications. VeloceRF seamlessly interfaces to leading EDA platforms in the layout, schematics, LVS, parasitic extraction, and signoff phases. It assists in efficient and compact floor-planning and provides highly accurate electromagnetic models, S-parameters, and Rational Function Model (RFM) formats. These models are silicon-verified up to 110 GHz.
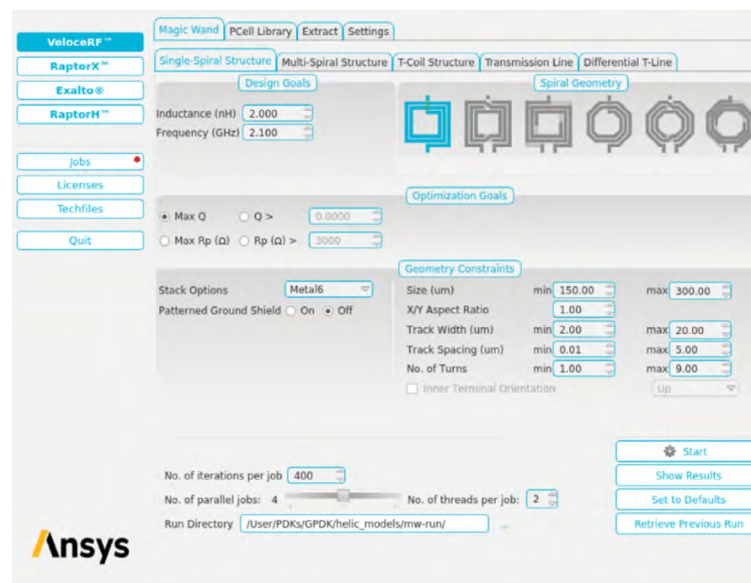


Figure 1: Device synthesis GUI in Ansys VeloceRF

# / The Most Sophisticated Inductor and Transformer Topologies

VeloceRF parametric cells allow you to build the most sophisticated devices by manipulating a long list of geometrical parameters available for each topology. Single-ended, differential square, and octagonal spirals, baluns, transformers, and T-coils can be customized to track width and spacing, stacking profile, number of turns, terminal orientation and position, inner and outer size, and presence of a patterned ground shield. The parametric cells are DRC-clean by design and support the most complex dummy fill patterns (billions of dummy tiles) down to 3nm in order to satisfy foundry Design-for-Manufacturability (DfM) constraints.
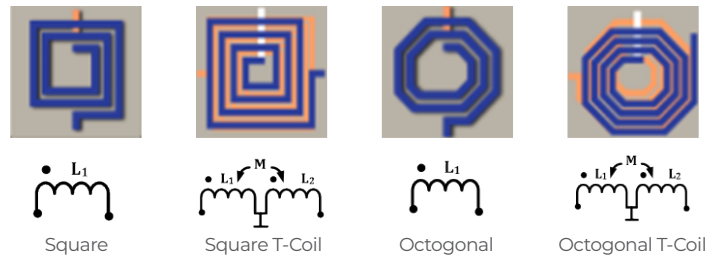
## Single-ended spiral topologies



Square     Square T-Coil     Octogonal     Octogonal T-Coil

Figure 2: Single-ended spiral topologies that can by synthesized with VeloceRF

## Differential spiral topologies



Square     Square Series     Octogonal     Octogonal Series
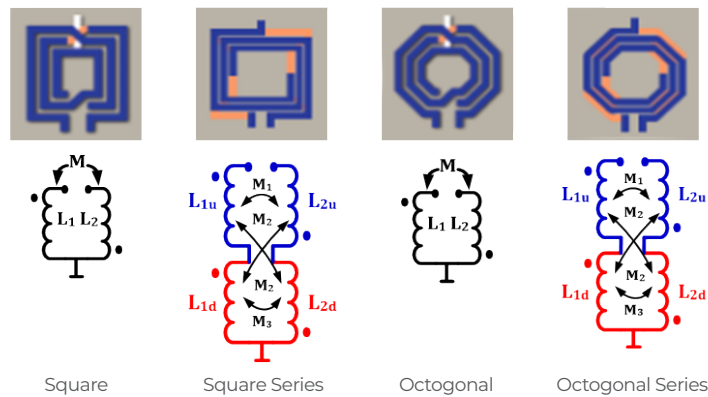
Figure3: Differential spiral topologies that can be synthesized with VeloceRF

## Transformer/Balun topologies



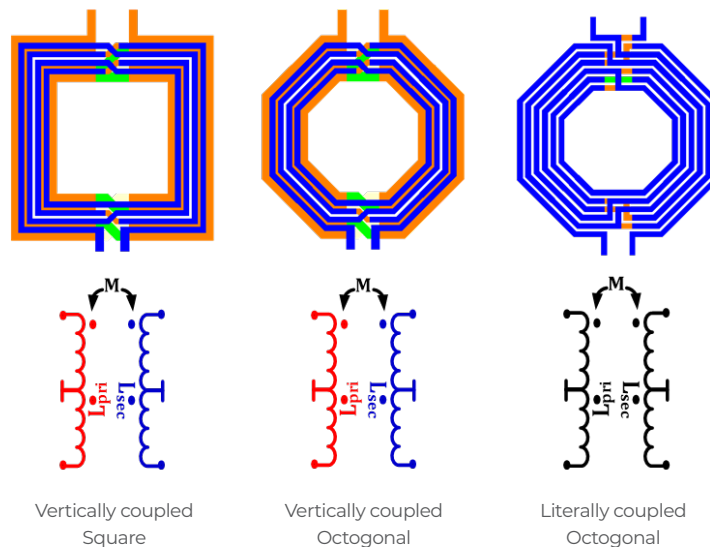Vertically coupled Square     Vertically coupled Octogonal     Literally coupled Octogonal

Figure 4: Transformer/balun topologies that can be synthesized with VeloceRF

# Synthesize Millimeter-wave Devices for Nanometer CMOS in Seconds

Ansys VeloceRF provides silicon-proven accuracy to mm-wave frequencies. A broad variety of transmission line structures supports a LEGO®-like approach to design, including microstrip lines, co-planar shielded and double-shielded waveguides, striplines, etc. Similarly to inductor parametric cells, the transmission line parametric cells are DRC-clean by design.

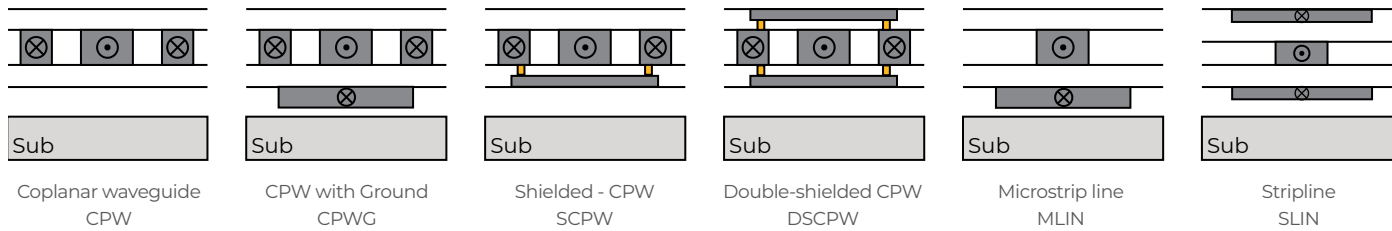## Single-ended transmission line topologies



| Coplanar waveguide CPW | CPW with Ground CPWG | Shielded - CPW SCPW | Double-shielded CPW DSCPW | Microstrip line MLIN | Stripline SLIN |

Figure 5: Single-ended transmission line topologies that can be synthesized with VeloceRF

## Defferential transmission line topologies



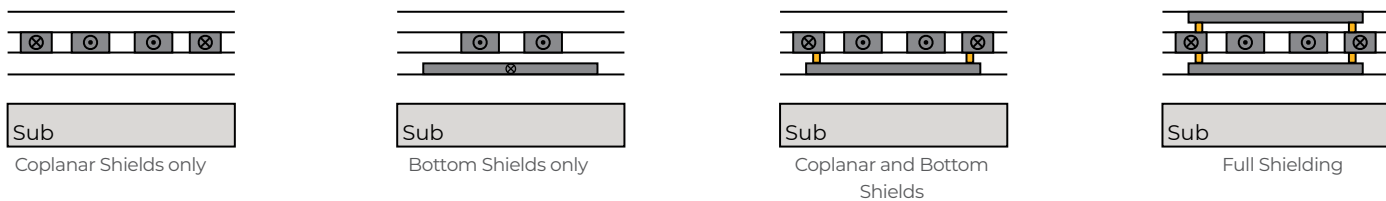| Coplanar Shields only | Bottom Shields only | Coplanar and Bottom Shields | Full Shielding |

Figure 6: Differential transmission line topologies that can be synthesized with VeloceRF

# Build and model your most complex bus topologies and transmission lines with VeloceRF

VeloceRF includes a powerful module that automates the design of transmission lines and buses of arbitrary complexity. Now it is easier than ever to design and model any complex bus topology with any number of signal, power and ground lines, and ground shields that are solid or perforated. VeloceRF reduces design and modeling time of complex buses from several weeks to a few hours.
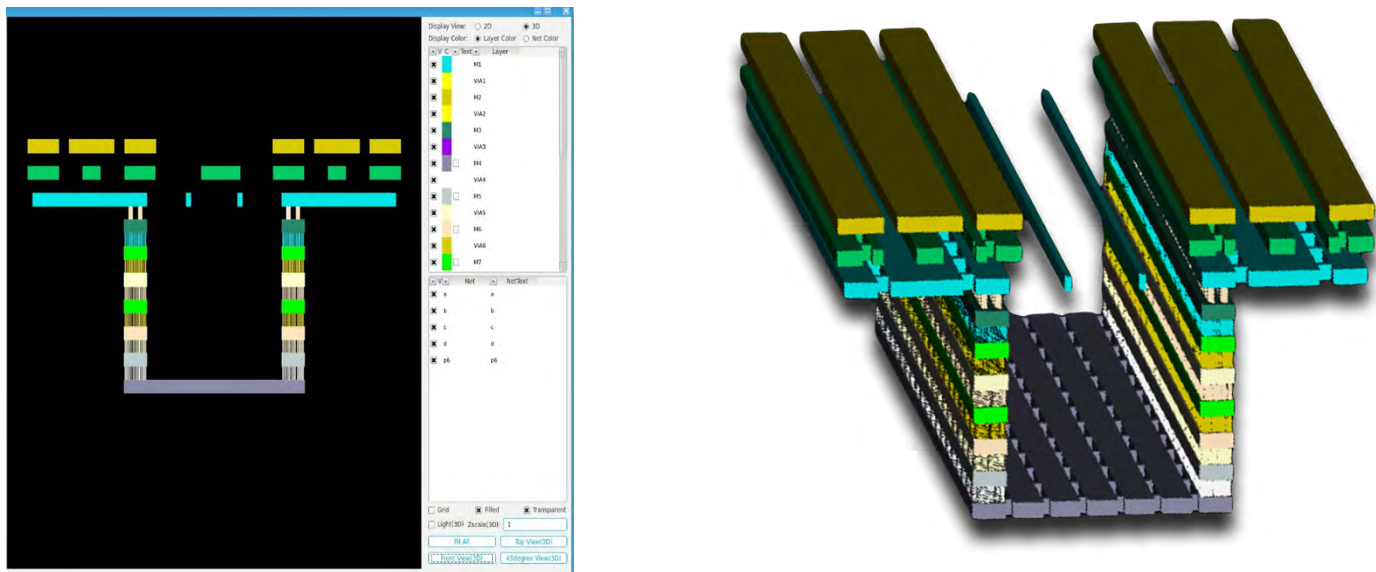


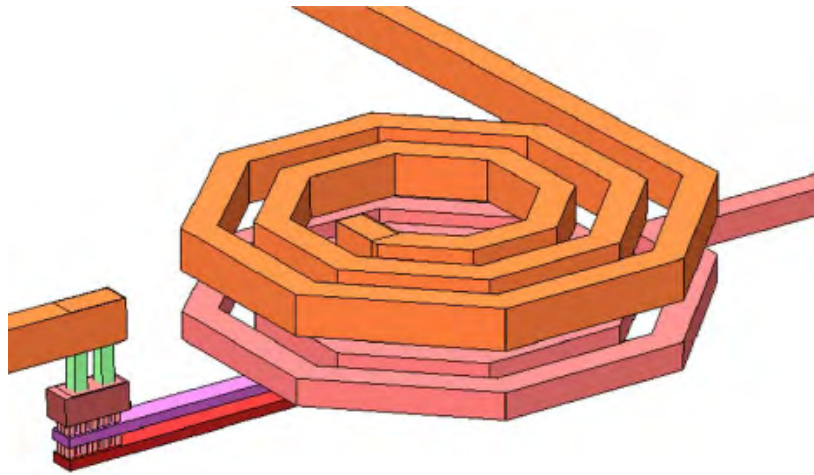Figure 7: VeloceRF Bus Builder cross-section editor and 3D view of bus topology

Figure 8: 3D view of a T-coil inductor

## / Minimize Your Silicon Real-estate by Building Smaller Passive Devices

Inductor size can impact overall die size. VeloceRF helps you design smaller devices using optimization criteria and geometry constraints according to available silicon real estate. Combine VeloceRF with Ansys RaptorX™ to calculate inductor-to-inductor and inductor-to-routing coupling, build the optimum floorplan, and eliminate crosstalk-related failures.

## / Accelerate Circuit Simulation Using the Most Appropriate Model Output from VeloceRF

VeloceRF generates passive, causal models in S-parameter format (for AC, harmonic-balance, and SP analyses) and Rational Function Models (RFM) format suitable for transient, shooting, and noise analyses. Circuit simulation is no longer a challenge with VeloceRF models.
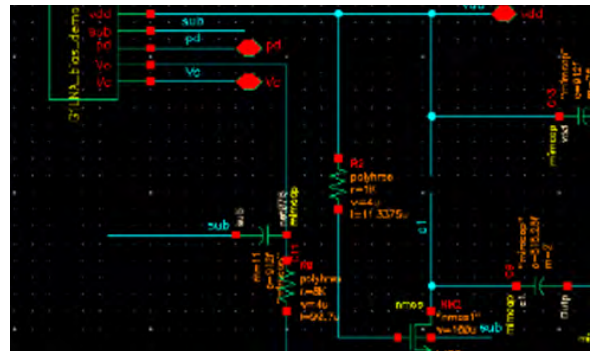


## / Compatible with All IC Design Platforms and Flows

VeloceRF works seamlessly with all leading custom IC design platforms, DRC, LVS, and parasitic extraction tools. The passive devices synthesized with VeloceRF are DRC-clean and DFM-compatible by design. Various automations eliminate the need for manual intervention during LVS, parasitic extraction, and circuit simulation with VeloceRF devices.
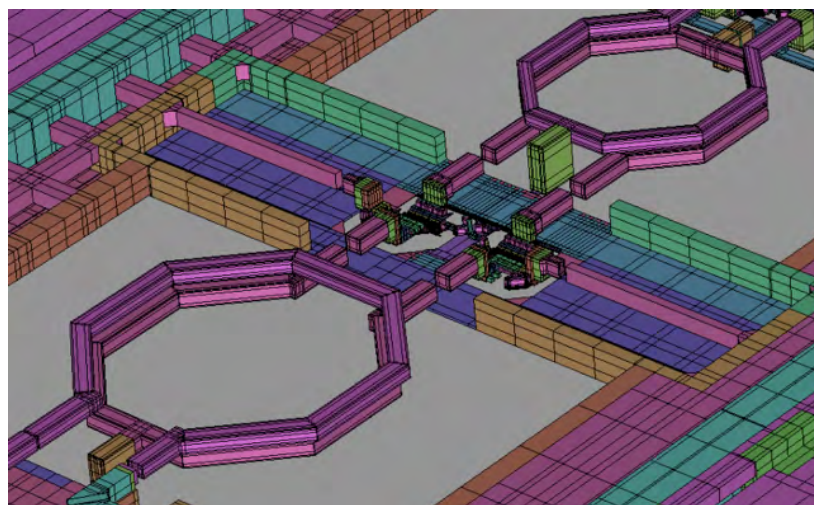

Figure 9: 3D mesh of Low-Noise Amplifier (LNA)

## / Silicon-proven EM Accuracy

VeloceRF works with any silicon process down to 3nm and is powered by the certified best-in-class RaptorX electromagnetic solver. Ansys VeloceRF technology and flow has been certified by various EDA industries and foundries.

- Synopsys, Ansys and Keysight Accelerate 5G/6G SoC Designs with New mmWave Reference Flow for TSMC Process Technology. To know more Click Here

- Ansys and TSMC Collaborate to Deliver Multiphysics Design Methodology for Wireless Chips. To know more Click Here

- Samsung Adopts Ansys' Simulation Portfolio to Create Semiconductor Designs to Optimize High-Speed Connectivity. To know more Click Here

## / Fundamental Block of the Ansys On-chip Electromagnetic Simulation Workflow

VeloceRF is the entry point to a complete EM-aware design methodology that starts with fast constraint-driven synthesis of inductive devices and complex transmission line structures. VeloceRF massively accelerates inductance modeling compared to conventional electromagnetic simulation. Synthesize the optimal inductor, balun, T-coil, or transmission line in a few minutes and eliminate unnecessary iterations that usually take hours or even days.

With VeloceRF IC, designers can drive passive device synthesis through a user-friendly GUI and run the complete design flow from pre-layout simulation to LVS and parasitic extraction with the accuracy of the VeloceRF electromagnetic models, all inside the standard IC design platform.

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