



AN APPLICATION BRIEF FROM ANSYS, INC.

## Automated Decoupling Capacitor Analysis Using SIwave PI Advisor

### ABSTRACT

When working in deep sub-micron technologies, designers are left with the task of reducing the cost of their design to meet tight design schedules within the provided budget. Optimization of today's high-volume printed circuit boards and packages is mostly based on different capacitor models, capacitor price and different number of capacitors, and it must be achieved without compromising the design's signal-and power-integrity performance. PI Advisor™, an add-on option introduced in SIwave® 5.0, significantly improves engineering productivity by automating decoupling capacitor selection, placement and optimization for printed circuit boards and packages.

### PRODUCTS USED

PI Advisor - SIwave 5.0 and above

### KEYWORDS

Decoupling capacitors, PCB optimization, impedance mask, ports, loop inductance, scheme, cost, package.

### PROBLEM DESCRIPTION

The primary goal of SIwave's PI Advisor is to find a set of decoupling capacitor assignments that satisfy the impedance mask specified by the user at the minimum cost. The technology allows the user to impose various additional constraints on the optimization problem, such as the total number of capacitors, types of caps, and total dollar cost. The most typical constraints used during a PI Advisor simulation are capacitor price, total number of capacitors, desired network impedance, types of capacitors and capacitor placement. These are incorporated into the optimizer's overall cost function as a weighted penalty. PI Advisor allows a user to perform two sets of analysis. A Simple PI lumped analysis used in pre-layout stage provides the engineer with a quick calculation for determining capacitor values and placement within user-defined regions. Based on the user-defined impedance mask, it determines the lumped circuit equivalent of all the capacitors on a board or package and can be used to develop the best candidate capacitors for a given design. In addition, it will automatically determine the best type and number of capacitors given a frequency-dependent impedance mask. The SIwave built-in capacitor library browser provides an intuitive and easy-to-use graphical interface for selecting and analyzing various capacitors in the vendor-provided library. All capacitor models have been provided by the manufacturer and are represented as touchstone models.

The most accurate simulation involves the presence of a printed circuit board or package, and it utilizes accurate frequency-dependent capacitor models (touchstone) during the post-layout simulation. In addition, the impact of the capacitor's physical location and mounting technique are captured by the full-wave SIwave extraction engine. Multiple bill of materials (BOM) schemes are available and can be applied to a final PCB or PNG design. PI Advisor can perform loop inductance analyses and plot 3-D bar graphs representing loop inductance values per each capacitor in a user-defined region, giving an immediate, intuitive understanding of each capacitor's effectiveness.

In the example below, a functional design with all capacitors placed was used to perform a PI Advisor simulation to reduce the capacitor cost and counts without impacting design performance. A selected number of user-defined ports will be included in decoupling capacitor optimization analysis. Based on the user-defined set of goals and constraints, a specific number of S-parameter capacitor candidates can be selected for optimization analysis. Impedance profile specified by the IC manufacturer has been met with a smaller number of capacitors without compromising design performance. A user-selected solution scheme can be applied to an overall design, resulting in optimized printed circuit board design.

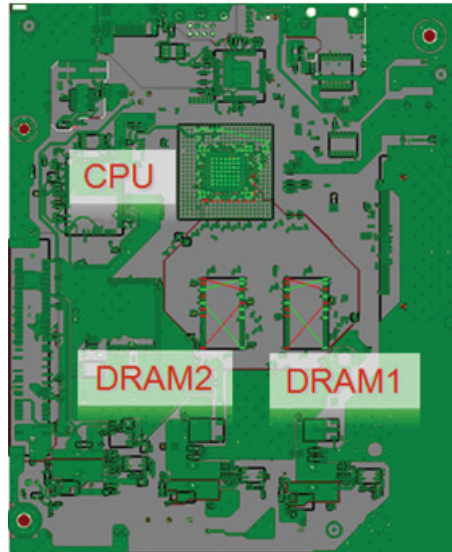


Figure 1: Fully functional PCB design. Designer has a task of minimizing the target impedance profile between CPU and DRAM 1 and DRAM2.

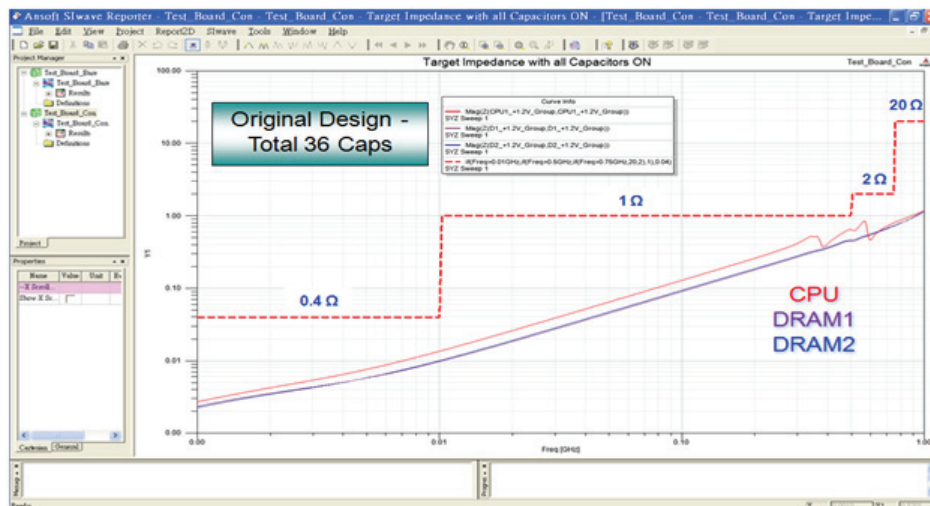


Figure 2: Original PCB design has 36 different capacitors placed in the region of interest between CPU and DRAM1 and DRAM2. The question is: Can similar design performance be obtained with fewer, less-costly capacitors?

Name	Goodness of Fit	Price (\$)	Num Caps	Cap Types
Scheme 8	1	0.15	15	13
Scheme 7	0.994484	0.17	17	15
Scheme 6	0.993107	0.16	16	14
Scheme 5	0.987651	0.15	15	13
Scheme 4	0.981267	0.14	14	12
Scheme 3	0.973381	0.11	11	10
Scheme 2	0.956865	0.18	18	16
Scheme 1	0.953822	0.14	14	12
Scheme 0	0.941352	0.1	10	9

Apply Scheme to Design    Export Scheme BOM...

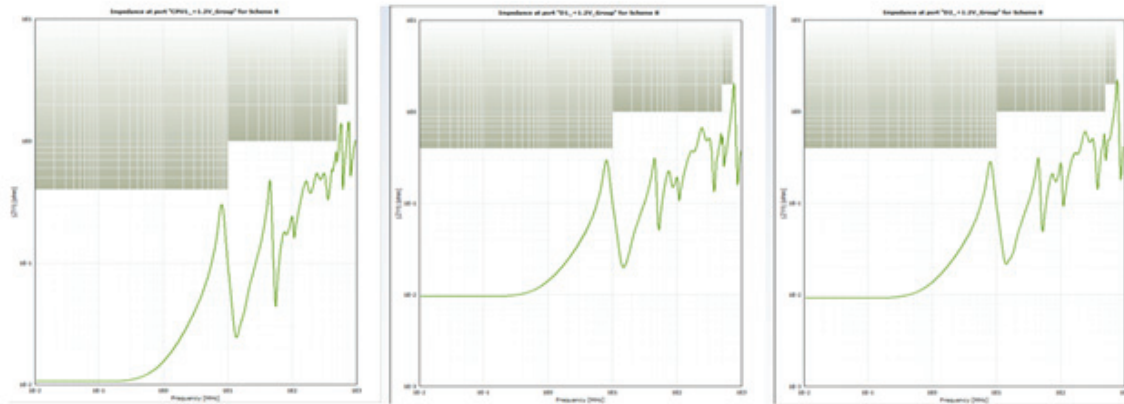


Figure 3: Based on all available capacitor candidates, eight different solution schemes are offered for a user to apply to optimized PCB design. Impedance mask can be displayed for each port used in optimization simulations.

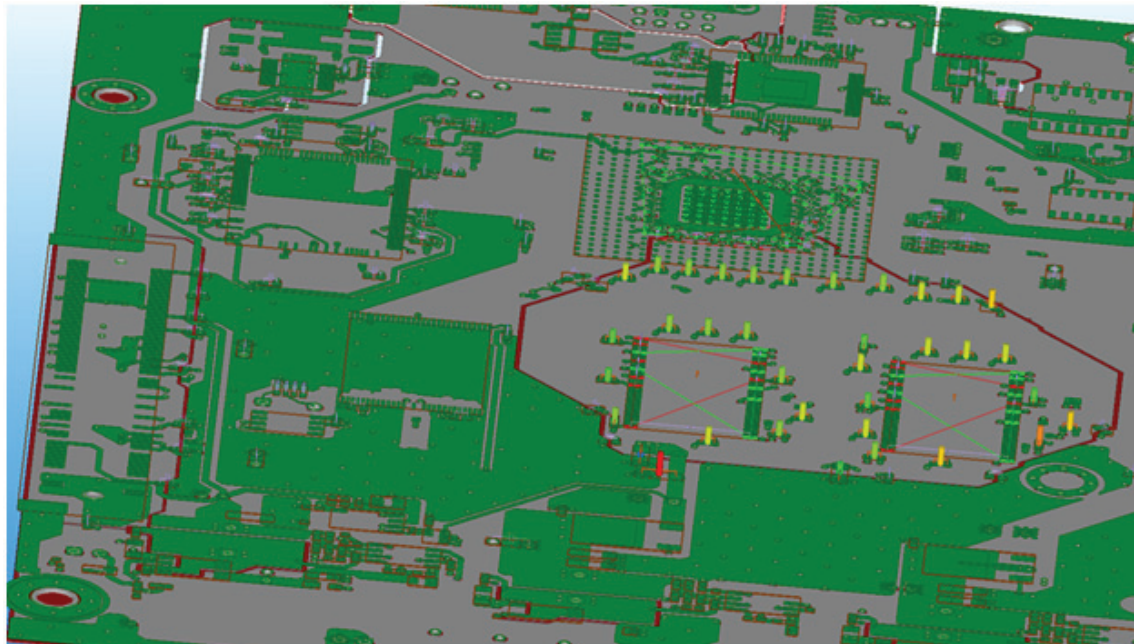


Figure 4: Bar graphs representing intuitive plot of loop inductance values for each capacitor placed between ICs of interest

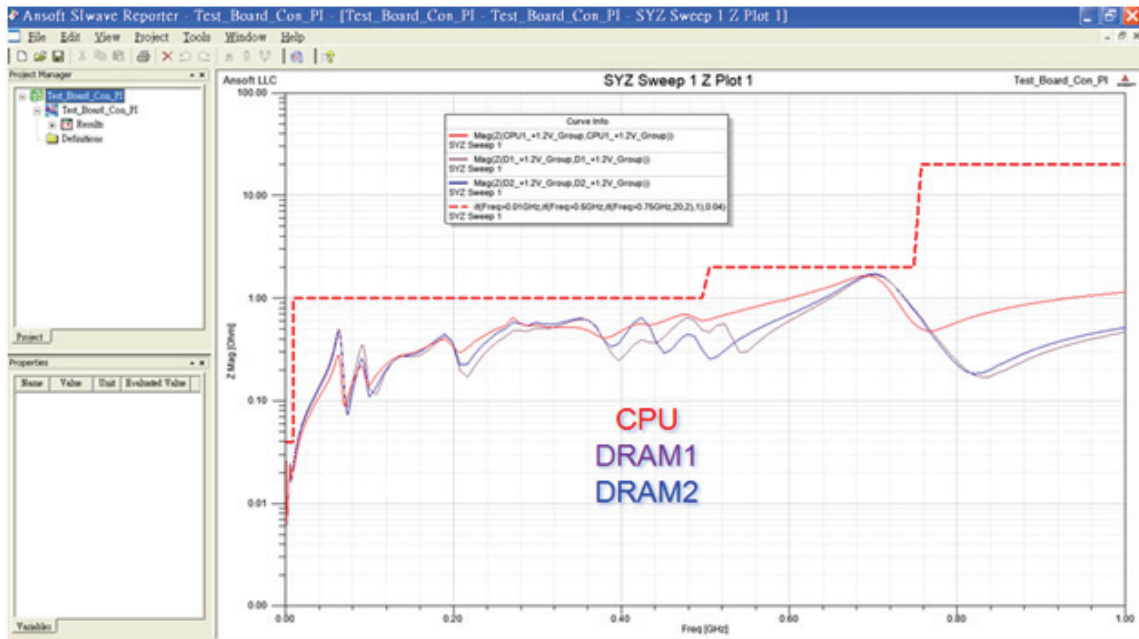


Figure 5: New and optimized result meets target impedance using fewer and less costly capacitors.

## CLOSING SUMMARY

In the example, the SIwave PI Advisor add-on option is used to optimize printed circuit board design based on the capacitor count, capacitor price and capacitor location. Different solution schemes based on capacitor count, price and capacitor types will be available to apply to a functional design. With all these different constraints included in PI Advisor full-wave simulation, a more robust PCB/PNG design can be achieved without compromising its signal- and power-integrity performance.



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