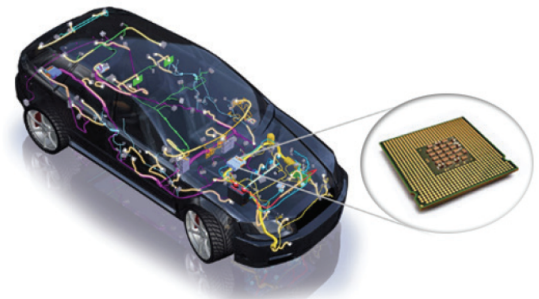


Ansys medini solutions for ISO 26262 in Semiconductors

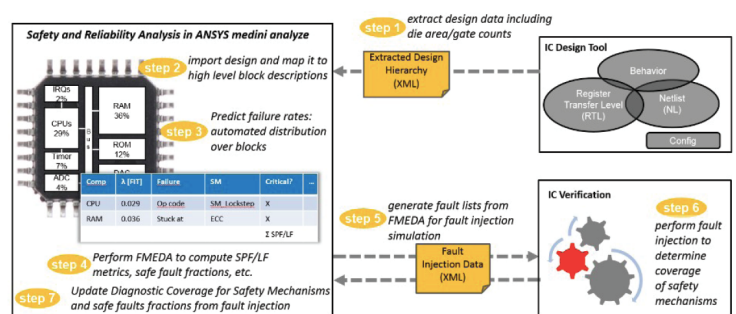
Ansys medini analyze ensures semiconductor performance in the automotive domain with dedicated ISO 26262 support. With the advent of ISO 26262, hardware designs must be analyzed for automotive functional safety. Our customers report up to a 55% decrease in efforts required for functional safety analysis and a similar decrease in time-to-market. Additionally, any inconsistencies in the functional safety analysis work products are eliminated, and confirmation reviews and assessments are accelerated.

Analysis methods to be applied include qualitative methods (e.g., FMEA, qualitative FTA), quantitative analysis (e.g., failure rate prediction; diagnostic coverage, residual and latent faults analysis, FMEDA, FTA,), as well as dependent failure analysis. These methods need to be carried out at various levels ranging from IP Design, parts and sub-parts of integrated components, up to subsystems and systems. medini analyze supports such integrated safety analysis.

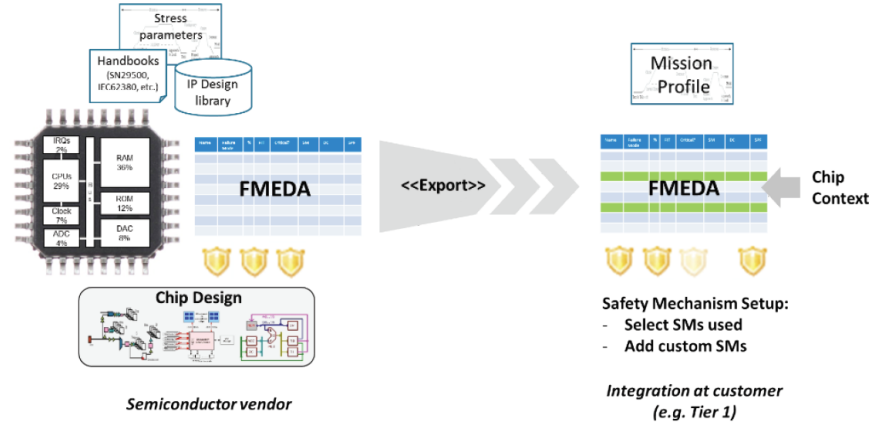
- Functional Safety Requirements.
- Failure Mode and Effects Analysis (FMEA).
- Hardware Diagnostic Coverage Metrics (FMEDA).
- Safety Mechanism Design.
- Connection to Fault Injection & Simulation.
- Fault Tree Analysis (FTA).
- Dependent Failure Analysis.
- Change Management & Impact Analysis.



ISO PAS 19451 for semiconductors requires failure mode analysis with detailed cause/effects of a design down to the sub-part level. Analysis (e.g., HW metrics) is done with assumptions of safety goal violations, base failure rates and distributions and diagnostic coverage (DC) rates of safety mechanisms. Such DC rates are validated by fault injection using third party tools.



Results of the safety analysis of the semiconductor design need to be provided by the semiconductor vendor to its customer, usually working on the system level and being responsible for the safety analysis at this level. It is essential to provide such analysis results in a configurable way, so that the system integrator can provide final stress parameters as part of a mission profile for the calculation of base failure rates, select and configure safety mechanisms, and provide additional safety mechanisms.



/ Ansys medini analyze Enterprise for Semiconductors Package includes:

1. Seamless exchange of IP design between hardware designers and safety analyst.
2. Derivation of base failure rates for a hardware design.
3. Automatic determination of failure distributions based on design data (e.g., die area, gate counts).
4. FMEA, FMEDA and FTA analysis based on the hardware design, incl. SPF/LF metrics, safe fault fractions.
5. “Closed loop” update of analysis data while design changes.
6. Reuse and adaptation of FMEDA data from previous designs.
7. Export of configurable FMEDA result data for handover of safety data to integrators.

Failure Rate Distribution derived from IP Design

ID	Name	Total Failure Rate	Total Safety Related Failure Rate	Total/Net Safety Related Failure Rate	Total/SPF Failure Rate	SPF Target	SPF Metric	Total LF Failure Rate	LF Target	LF Metric	Observation Points	Total Soft Error Rate
S019	Prevent DMA Descriptor Address Completion	0.011773	0.011773	0.0	6.5355E-4	99.0	94.4	0.0	90.0	100.0	0.0	0.0
S020	Prevent DMA Descriptor WriteData Completion	0.011773	0.011773	0.0	6.2071E-4	99.0	94.0	0.0	90.0	100.0	0.0	0.0
S021	Prevent DMA Data Buffer Address Completion	0.011773	0.011773	0.0	4.2408E-4	99.0	95.0	0.0	90.0	100.0	0.0	0.0

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